

The D2692 UART IP Core offers more

The D2692 is a Dual UART Core software compatible with the SC26C92, SCC2692 and SCN2681. But on the contrary to it, DCD's IP Core offers additional features and deeper FIFOs, like 8 character receiver, 8 character transmit FIFOs, watch dog timer for each receiver, mode register 0, extended baud rate, programmable receiver and transmitter interrupts.

The D2692 Dual Universal Asynchronous **of September 2013.**thBytom, 5

Receiver/Transmitter is a communication device that provides two full-duplex asynchronous receiver/transmitter channels in just one single package. DCD's IP Core interfaces directly with microprocessors and may be used in a polled or interrupt driven system, furthermore provides modem and DMA interface. The operating mode and data format of each channel can be programmed independently. -

Additionally, each receiver

and transmitter can select its operating speed

- says Jacek Hanke, DCD's CEO -

as one of 27 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock

. The opportunity to program independently the operating speed of the receiver and transmitter, denotes the UART particularly attractive for dual-speed channel applications like eg clustered terminal systems.

Every receiver is being equipped with fifo to minimize the potential of receiver over-run and to reduce interrupt overhead in interrupt driven systems. Moreover, the D2692 UART IP Core ensures a flow control capability, to disable a remote DUART transmitter, when the receiver buffer is full. To make this design even more functional, there've been added multipurpose 7-bit input port and a multipurpose 8-bit output port. They can be used as general purpose I/O ports or can be assigned to specific functions (eg clock inputs or status/interrupt outputs) under program control.

More information:

Each FIFO can be programmed for four different interrupt levels

- Watch dog timer for each receiver
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- Power down mode
- Receiver timeout mode

Information about Digital Core Design:

Digital Core Design is a leading Intellectual Property (IP) Core provider and System-on-Chip (SoC) design house. The company was founded in 1999 and since the early beginning has been considered an expert in IP Core architecture improvements. Thousands of customers became convinced by our unique solutions and billions of people worldwide use our technology in USBs, MP3 players, mobile phones and many other applications.

The innovativeness of DCD's IP solutions has been confirmed by over 500 licenses sold to over 300 customers worldwide, such as: INTEL, SIEMENS, PHILIPS, TOYOTA, OSRAM, GENERAL ELECTRIC, SILICON GRAPHICS, RAFAEL, SAGEM or GOODRICH.

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